CLAIMS

1. A process for transmitting at given instants digital signals on a bus, said digital signals being transmitted on the bus selectively in a non-encoded format and in an encoded format, comprising comparing a signal to be transmitted on the bus for an instant of said given instants with a signal transmitted on the bus for a preceding instant among said given instants so as to minimize switching activity on the bus, wherein said operation of comparing is carried out bit by bit in orderly sequence so as to identify, in the context of said signal to be transmitted on the bus at an instant of said given instants and of said signal transmitted on the bus for the preceding instant among said given instants, a first set of bits that are not changed and a second set of bits that are changed; and a decision whether to transmit said signals on the bus in non-encoded format and in encoded format is taken limitedly to the bits of said second set of bits.

2. The process according to claim 1, further comprising identifying, in the context of said orderly sequence, at least one marker bit that separates the bits of said first set from the bits of said second set.

3. The process according to claim 1 wherein said operation of comparing is carried out starting from a bit with a least probability of change.

4. The process according to claim 1, wherein said operation of comparing is carried out starting from a most significant bit.

5. The process according to claim 1 wherein said operation of comparing is carried out starting from a least significant bit.

6. The process according to claim 1 wherein said operation of comparing is carried out starting from a given bit, exploring other bits subjected to comparison moving in a given direction.

7. The process according to claim 1 wherein said operation of comparing is carried out starting from at least one given bit, exploring other bits subjected to comparison moving in opposite directions.

8. The process according to claim 1, further comprising transmitting, in non-encoded format, a first bit of said signal to be transmitted on the bus.

9. The process according to claim 1, further comprising encoding integrally, in view of transmission on the bus, said signal to be transmitted on the bus if said comparison operation reveals that a first bit considered in said orderly sequence is changed.

10. The process according to claim 1, further comprising transmitting on the bus the bits of said first set always in non-encoded format.

11. The process according to claim 1, wherein said encoded format is obtained by inverting the bits of the signal in non-encoded format

12. The process according to claim 1, further comprising associating with said digital signals an additional signal that is able to assume, at said given instants, different logic values according to whether the digital signal to which it is associated is transmitted in said non-encoded format and, at least in part, in said encoded format, respectively, so that said additional signal is able to modify a logic value between successive instants of said given instants;

detecting, for said digital signals, occurrence of a condition in which transmission on said bus in said non-encoded format and in said encoded format are able to give rise to an identical switching activity on the bus; and

deciding whether the signal to be transmitted on the bus at a given instant is to be transmitted in said non-encoded format or in said at least partially encoded format so as to cause the additional signal associated with said signal to be transmitted on the bus at a given instant to keep the logic value with respect to the logic value assumed by the additional signal associated with the signal transmitted on the bus for the preceding instant among said given instants.

13. The process according to claim 1, further comprising determining a distance between said signal to be transmitted on the bus at an instant among said given instants and the signal transmitted on the bus for the preceding instant among said given instants.

14. The process according to claim 13 wherein said distance is determined as a Hamming distance.

15. An encoder for transmitting at given instants on a bus digital signals selectively in a non-encoded format and an encoded format, the encoder comprising:

a comparison module for comparing a signal to be transmitted on the bus for an instant of said given instants with a signal transmitted on the bus for the preceding instant among said given instants, and generating at least one corresponding decision signal; and

a transmission-driving module for driving transmission of said signals on the bus in non-encoded format and in encoded format according to said decision signal so as to minimize a switching activity on the bus,

wherein said comparison module comprises a logic network that is able to compare bit by bit, in orderly sequence, said signal to be transmitted on the bus at an instant of said given instants and said signal transmitted on the bus for the preceding instant among said given instants, so as to identify a first set of bits that are not changed and a second set of bits at least some of which are changed; and

said transmission-driving module is configured for driving the transmission of said signals on the bus in non-encoded format and in encoded format limitedly to the bits of said second set of bits.

16. The encoder according to claim 15 wherein said logic network is configured to compare signals bit by bit, starting from a bit with a least probability of change.

17. The encoder according to claim 15 wherein said logic network is configured to compare signals bit by bit, starting from a most significant bit.

18. The encoder according to claim 15 wherein said logic network is configured to compare signals bit by bit, starting from a least significant bit.

19. The encoder according to claim 15 wherein said logic network is configured to compare signals bit by bit starting from a given bit, exploring other bits subjected to comparison, moving in a given direction.

20. The encoder according to claim 15 wherein said logic network is configured to compare signals bit by bit starting from at least one given bit, exploring other bits subjected to comparison, moving in opposite directions.

21. The encoder according to claim 15 wherein said at least one transmission-driving module is configured to drive transmission of a first bit of said signal to be transmitted on the bus in non-encoded format.

22. The encoder according to claim 15 wherein said at least one transmission-driving module is configured to drive transmission of said signal to be transmitted on the bus in integrally encoded format, if said logic network indicates that a first bit considered in said orderly sequence is changed.

23. The encoder according to claim 15 wherein said at least one transmission-driving module is configured for transmitting on the bus the bits of said first set always in a non-encoded format.

24. The encoder according to claim 15, further comprising an inverter circuit for generating said encoded format.

25. The encoder according to claim 15, further comprising:

a module for associating with said digital signals an additional signal that is able to assume, at said given instants, different logic values according to whether the digital signal to which it is associated is transmitted in said non-encoded format or, at least in part, in said encoded format, respectively, so that said additional signal is able to modify its logic value between successive instants of said given instants; and

a module for detecting, for said digital signals, an occurrence of a condition in which transmission on said bus in said non-encoded format and in said encoded format are able to give rise to an identical switching activity on the bus, wherein said transmission-driving module is configured to drive transmission of said signals on the bus in said non-encoded format and in said at least in part encoded format so as to cause the additional signal associated to said signal to be

transmitted on the bus at a given instant to keep a logic value with respect to a logic value assumed by the additional signal for transmission on the bus for the preceding instant among said given instants.

26. The encoder according to claim 15, further comprising a module for calculating a distance between said signal to be transmitted on the bus at an instant among said given instants and the signal transmitted on the bus for the preceding instant among said given instants.

27. The encoder according to claim 26 wherein said at least one module for calculating a distance comprises at least one module for calculating a Hamming distance.

28. A decoder for receiving digital signals transmitted on a bus , comprising:

a decoding logic configured to identify, in the context of each digital signal received, at least one marker bit that separates a first set of bits from a second set of bits; and

a logic reconstruction network for reconverting from an encoded format to a non-encoded format the bits of said second set.

29. The decoder according to claim 28 wherein said decoding logic is configured to identify said at least one marker bit as a bit of said digital signals with a least probability of change.

30. The decoder according to claim 28 wherein said decoding logic is configured to identify said at least one marker bit as a most significant bit of said digital signals.

31. The decoder according to claim 28 wherein said decoding logic is configured to identify said at least one marker bit as a least significant bit f said digital signals.

32. The decoder according to claim 28 wherein said decoding logic is configured to identify said at least one marker bit as a starting bit for exploring said digital data, carried out moving in a given direction.

33. The decoder according to claim 28 wherein said decoding logic is configured to identify said at least one marker bit as a starting bit for exploring said digital data, carried out moving in opposite directions.

34. The decoder according to claim 28 wherein the decoder is configured to assume as transmitted in non-encoded format a first bit of said digital signals.

35. The decoder according to Claim 28wherein the decoder is configured to assume a larger of the first and second set of bits as transmitted in said non-encoded format.

36. The decoder according to claim 28 wherein said logic reconstruction network reconverts said digital signals from said encoded format to said non-encoded format by means of logic inversion of bits subjected to encoding.

37. A computer program product directly loadable into the memory of a computer and comprising software code portions for : comparing a signal to be transmitted on a bus for an instant of given instants with a signal transmitted on the bus for a preceding instant among said given instants so as to minimize

switching activity on the bus, wherein said operation of comparing is carried out bit by bit in orderly sequence so as to identify, in the context of said signal to be transmitted on the bus at an instant of said given instants and of said signal transmitted on the bus for the preceding instant among said given instants, a first set of bits that are not changed and a second set of bits that are changed; and a decision whether to transmit said signals on the bus in non-encoded format and in encoded format is taken limitedly to the bits of said second set of bits.

38. A computer program product directly loadable into the memory of a computer and comprising software code portions for:

comparing a signal to be transmitted on a bus for an instant of given instants with a signal transmitted on the bus for a preceding instant among said given instants, and generating at least one corresponding decision signal; and

driving transmission of said signals on the bus in non-encoded format and in encoded format according to said decision signal so as to minimize a switching activity on the bus,

wherein comparing the signals comprises comparing bit by bit, in orderly sequence, said signal to be transmitted on the bus at an instant of said given instants and said signal transmitted on the bus for the preceding instant among said given instants, so as to identify a first set of bits that are not changed and a second set of bits at least some of which are changed; and

said transmission-driving module is configured for driving the transmission of said signals on the bus in non-encoded format and in encoded format limitedly to the bits of said second set of bits..

39. A computer program product directly loadable into the memory of a computer and comprising software code portions for decoding an encoded digital signal by:

identifying, in the context of each digital signal received, at least one marker bit that separates a first set of bits from a second set of bits; and

reconverting from an encoded format to a non-encoded format the bits of said second set.

40. A method of encoding a digital signal, comprising:

transmitting a first signal;

comparing a second signal to the first signal;

identifying a first set of bits in the second signal that are not changed and a second set of bits in the second signal at least some of which are changed based on the comparison to the first signal;

processing the first set of bits in a first manner;

processing the second set of bits in a second manner; and

transmitting the processed first and second sets of bits.

41. The method of claim 40, further comprising transmitting the first signal on a bus.

42. The method of claim 40 wherein comparing the second signal to the first signal comprises sequentially comparing bits of the second signal with corresponding bits of the first signal until the comparison does not yield a match and the first set of bits comprises the bits that yielded a match.

43. The method of claim 42 wherein comparing the second signal with the first signal comprises starting the comparison with a most significant bit of the signals.

44. The method of claim 40 wherein the first manner of processing comprises transmitting the first set of bits in a non-encoded format and the second

manner of processing comprises transmitting at least part of the second set of bits in an encoded format.

45. The method of claim 40 wherein the second manner of processing comprises encoding the second set of bits using a bus-inverter encoding process.

46. The method of claim 40 wherein the first manner of processing comprises encoding the first set of bits using a bus-inverter encoding process.

47. The method of claim 40 wherein the first set of bits is an empty set.

48. The method of claim 40 wherein the second set of bits is an empty set.

49. The method of claim 40, further comprising identifying a first subset of the second set of bits and a second subset of the second set of bits and the manner of processing the second set of bits comprises transmitting the first subset of bits in a non-encoded format and transmitting the second subset of bits in an encoded format.

50. The method of claim 40, further comprising generating a control signal based on the comparison and transmitting the control signal.

51. A method of decoding a digital signal, comprising:
receiving a digital signal comprising a plurality of data bits;
identifying a marker bit in the plurality of data bits;

identifying first and second sets of data bits in the plurality of data bits based at least in part on the identity of the marker bit;

processing the first set of data bits in a first manner; and

processing the second set of data bits in a second manner.

52. The method of claim 51, further comprising receiving a control signal wherein the processing of the second set of data bits is controlled based at least in part on the control signal.